VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

On Page 3, the second paragraph starting at Line 13 is modified as follows:

The command signals chip select **$\overline{CS}$**, the row address strobe **$\overline{RAS}$**, column address strobe **$\overline{CAS}$**, and the write enable **$\overline{WE}$**, as well as the address bus A_0, A_1, ..., A_n are gated into the SDRAM during the rise of the internal clock **ICLK** from a first logic level (0) to a second logic level (1). The internal clock **ICLK** is the timing signal that is used to synchronize the transfer of the digital data from the cell array in the memory banks to the data input/output buffers and to the data bus DQ_0, ..., Dq_x. The internal clock **ICLK** is delayed or skewed by the delay d_1 of the input buffer **IBUF** plus the internal buffer **INTBUF**. Since the timing of the functions of the SDRAM are determined by the internal clock **ICLK**, the access time T_{acc} of the fetching or reading of the digital data can be no smaller than the clock skew d_1+d_2 plus the period of the internal clock **ICLK**. This forces the minimum time that data can be cycled from the SDRAM to be two external system clock **XCLK** periods. As computer system clocks are approaching transfer rates of 100Mhz, it is desirable that the access time T_{acc} of an SDRAM to be brought to one cycle of the external system clock **XCLK**. This means that the clock skew d_1+d_2 must be eliminated from the clock distribution system.

On Page 4, the last paragraph starting at Line 21 is modified as follows:

Figs. ~~1a and 1b~~2a and 2b show a schematic diagram and a timing diagram for the general structure of a CSD circuit. The external system clock **XCLK** is received by the input buffer **IBUF**. The output **IBO** of the input buffer **IBUF** is delayed by the delay $\mathbf{d_1}$. The output **IBO** of the input buffer **IBUF** is the input to the delay monitor circuit **DMC**. The delay monitor circuit **DMC** provides an output that is a delayed input signal **IBO** by a fixed amount that is usually the sum of the delay $\mathbf{d_1}$ of the input buffer **IBUF** and the delay $\mathbf{d_2}$ of the internal buffer **INTBUF**.

On Page 10, the first full paragraph starting at Line 7 is modified as follows:

An object of this invention is to provide an internal clock circuit in an integrated circuit that creates an internal clock signal that is synchronized with ~~from~~ an external system clock signal.

On Page 10, the third paragraph starting at Line 16 is modified as follows:

To accomplish at least one of these objects, as well as ~~and~~ other objects, a clock synchronizer circuit provides an internal clock signal for an integrated

circuit that is synchronized to an external system clock signal, such that the internal clock integrated is aligned with and has minimal skew from the external system clock signal. The clock synchronizer circuit has a plurality of serially connected delaying circuits to receive the external system clock signal and delay the external system clock signal by an incremental period of delay. The incremental period of delay is equal to the period of the external system clock signal. The clock synchronizer circuit further has a plurality of frequency divider circuits. The first frequency divider circuit of the plurality of frequency divider circuits is connected to receive the external system clock signal and to divide a frequency of the external system clock signal by a dividing factor and each remaining frequency divider circuits is connected to an output of one of the serially connected delaying circuits to divide a delayed external system clock signal by the dividing factor providing a plurality of divided external system clock signals. The clock synchronizer circuit also contains a plurality of clock synchronization delay circuits. Each clock synchronization delay circuit is connected to one of the plurality of frequency divider circuits to synchronize each divided external system clock signal to the external system clock signal. A logical combining circuit is connected to each of the plurality of clock synchronization circuits to combine the synchronized, divided external system clock signal to form the internal clock signal.

On Page 11, the third paragraph starting at Line 29 is modified as follows:

_____Each clock synchronization delay circuit is a synchronous mirror delay circuit. The synchronous mirror delay circuit has a buffer circuit connected to one of the frequency divider circuit to buffer, amplify and delay one of the delayed and divided external timing signals to create a first timing signal. A fixed delay circuit is connected to the buffer circuit to delay the first timing signal by a circuit delay factor that is a sum of a first delay factor and a second delay factor. The first delay factor is a delay time of the frequency divider circuit and the buffer circuit. A forward delay circuit measures a difference time period. The difference time period is the circuit delay factor subtracted from the period of the delayed and divided external timing signal. A mirror delay circuit is connected to the forward delay circuit and the buffer circuit to delay the first timing signal by the difference time period to create a second timing signal. An internal buffer circuit is connected to the mirror delay circuit to amplify, delay the second timing signal to create the synchronized, divided external system clock signal whereby a delay time of the internal buffer circuit is the second delay factor.

On Page 12, the second paragraph starting at Line 12 is modified as follows:

In a second embodiment of a clock synchronizer circuit that provides an internal clock signal for an integrated circuit that is synchronized to an external system clock signal, such that the internal clock signal integrated is aligned with and has minimal skew from the external system clock signal has a single

frequency divider circuit that receives the external system clock signal and divides its frequency by a dividing factor to form a divided external clock signal. The first delaying circuit of a plurality of serially connected delaying circuits is connected to the frequency divider circuit to receive the divided external clock signal, and each of the remaining delaying circuits delays the delayed external clock signal by an incremental period of delay to form a plurality of delayed and divided external clock signals. The first clock synchronization delay circuit of a plurality of clock synchronization delay circuits is connected to the frequency divider circuit and each remaining clock synchronization delay circuit is connected to one of the plurality of serially connected delaying circuits to synchronize each delayed and divided external clock signal to the external system clock signal. A logical combining circuit combines the synchronized, delayed and divided external clock signals to form the internal clock signal.

On Page 24, the second paragraph starting at Line 13 is modified as follows:

The submultiple clocks **NCLK1**, and **NCLK2** are each buffered, amplified, and delayed in the input buffers **IBUF** the clock synchronous delay circuits **CSD1** and **CSD2** to create the output **IBO1** and **IBO2**. The outputs **IBO1** and **IBO2** of the input buffers **IBUF** the clock synchronous delay circuits **CSD1** and **CSD2** are delayed by the delay factor $\mathbf{d_1}$ respectively from the submultiple clocks **NCLK1**, and **NCLK2**. The outputs **IBO1** and **IBO2** of the input buffers **IBUF** the clock

synchronous delay circuits **CSD1** and **CSD2** are the inputs to the delay monitor circuits **DMC** from the submultiple clocks **NCLK1**, and **NCLK2**. The delay monitor circuits **DMC** from the submultiple clocks **NCLK1**, and **NCLK2** each provide an output that is the delayed input signal **IBO1** and **IBO2** by a fixed amount that is usually the sum of the delay factor $\mathbf{d_1}$ of the input buffers **IBUF** the clock synchronous delay circuits **CSD1** and **CSD2** and the delay factor $\mathbf{d_2}$ of the internal buffer **INTBUF**.

In the Claims:

The Claims are amended as follows:

18. (Amended) A synchronous dynamic random access memory to retain digital data, comprising:

a clock generator circuit connected between an external system clock distribution circuit and a plurality of banks of arrays of memory cells, an address circuit, a command circuit, a data control circuit, and a data input/output buffer to provide ~~a timing~~ an internal clock signal to synchronize operation of said synchronous dynamic random access memory, whereby certain operations must occur in time with minimal deviation from said an external system clock signal and whereby said clock generator includes at least one clock synchronizer circuit, comprising;